REMARKS

The Office Action dated June 6, 2004 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto. Claims 2-7 are allowed and claim 1 is presently pending and presented for consideration.

The Office Action withdrew the allowability of claim 1 because of newly discovered U.S. Patent No. 6,298,096 to Burgin. Claim 1 was rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,298,096 to Burgin. The rejection is traversed as being based on a reference that neither teaches nor suggests the novel combination of features clearly recited in independent claim 1.

Claim 1 recites a method for providing a data symbol having a first quadrature compensated data symbol (FQCDS), a second quadrature compensated data symbol (SQCDS), a first in-phase compensated data symbol (FICDS) and a second in-phase compensated data symbol (SICDS) to an inverse fast fourrier transform (IFFT) of a multicarrier quadrature modulator having an amplifier. A first subcarrier data symbol and a second subcarrier data symbol are available from a mapper and an alpha, an epsilon, and a gain are predetermined. The alpha, epsilon and gain are imbalance parameters. The method includes the steps of first quadrature compensating the data symbol based on the alpha, epsilon and gain to produce the FQCDS and second quadrature compensating the data symbol based on the alpha, epsilon and gain to produce the SQCDS. The method also includes the steps of first in-phase compensating the data symbol based on the alpha, epsilon and gain to produce the FICDS and second in-phase compensating the data symbol based on the alpha, epsilon and gain to produce the SICDS.

As will be discussed below, the cited prior art reference of Burgin fails to disclose or suggest the elements of any of the presently pending claims.

Burgin teaches a predistortion quadrature modulator which performs direct modulation of a signal at the frequency of transmission. The predistortion quadrature modulator operates in a transmission mode and a calibration mode. In the transmission mode, the signals to be transmitted are modulated according to normal operation and transmitted over a wireless link and in the calibration mode no signal is transmitted and the predistortion parameters are determined.

The predistortion quadrature modulator includes a digital predistortion block which pre-compensates the baseband transmission or calibration mode signals and converts them to analog form; a quadrature modulation block which represents the quadrature modulator including the imperfections which it introduces; an amplitude modulation (AM) detection block which uses an AM detection process to generate a baseband analog signal or to pass the transmission signal to the next stage and a parameter determination block which collects data samples and executes a series of calculations to determine a set of predistortion parameter for use in subsequent transmission mode operation.

The digital predistortion block includes four adjustable elements which are used to pre-compensate for errors introduced by circuit imperfections. The Q channel input to the digital predistortion block is coupled to the input of a crosstalk amplifier and the I channel input to the digital predistortion block is coupled to a sumner which sums the I channel input with the output of the crosstalk amplifier. The gain of the crosstalk amplifier is determined by a predistortion parameter K. The output of the sumner is coupled to a unity gain amplifier and the Q channel input is coupled to a gain distortion amplifier. The gain of the gain distortion amplifier is determined by the predisposition parameter G_q. The output of the unity gain amplifier and gain predistortion amplifier are coupled to respective D.C. offset sumners 118 and 120, wherein D.C. offset predistortion sumner 118 sums a D.C. offset signal determined by the predistortion

parameter b_i and D.C. offset predistortion sumner 120 sums a D.C. offset signal determined by the predistortion parameter b_q. The output of the D.C. offset gain predistortion sumners are coupled to digital-to-analog (D/A) converters that produce low frequency baseband analog signals which are coupled to the quadrature modulation block.

The outputs of the D/A converters are coupled to respective sumners 130 and 132 in the quadrature modulation block where the undesirable D.C. offset for the I channel is summed with the I channel signal and the undesirable D.C. offset for the Q channel is summed with the Q channel signal.

Applicant submits that Burgin simply does not teach or suggest each of the elements recited in claim 1. The Office Action states that Burgin teaches the steps of first quadrature compensation the data symbol as recited in claim 1 by first quadrature compensating the current data symbol based on the input of D.C. offset predistortion sumner 118 and 120, the input of sumners 130 and 132 and the gain controlled signal at the input of the crosstalk amplifier and the gain predistortion amplifier. The Office Action also states that Burgin teaches the steps of second quadrature compensation the data symbol as recited in claim 1 by second quadrature compensating the next data symbol based on the input of D.C. offset predistortion sumner 118 and 120, the input of sumners 130 and 132 and the gain controlled signal at the input of the crosstalk amplifier and the gain predistortion amplifier. Claim 1 in part recites that the data symbol include a first quadrature compensated data symbol (FQCDS), a second quadrature compensated data symbol (SQCDS), a first in-phase compensated data symbol (FICDS) and a second in-phase compensated data symbol (SICDS). Claim 1 also recites first quadrature compensating the data symbol based on the alpha, epsilon and gain to produce the FQCDS and second quadrature compensating the data symbol based on the alpha, epsilon and gain to produce

the SQCDS. According to the Office Action, Burgin teaches first quadrature compensating the current data symbol and second quadrature compensating the next data symbol. As such, it is clear that Burgin simply does not teach first and second quadrature compensating the same data symbol as recited in claim 1.

Furthermore, Applicant submits that Burgin, does not teach or suggest the steps of first quadrature compensating, second quadrature compensating, first in-phase compensating and second in-phase compensating as recited in claim 1. Although the Office Action states that Burgin teaches the steps of first quadrature compensating, second quadrature compensating, first in-phase compensating and second in-phase compensating as recited in claim 1, Burgin teaches a quadrature modulator which precompensates for errors introduced by the quadrature modulator by calculating offset adjustments to an I channel and a Q channel signal path, cross talk gain between the I channel and Q channel signal path and a gain offset adjustment between the I channel signal path and the Q channel signal path. Therefore, Applicant assert that the rejection under 35 U.S.C. 102 (e) should be withdrawn because Burgin simply does not teach or suggest each of the elements recited in claim 1.

As noted previously, claim 1 recites subject matter which is neither disclosed nor suggested in the prior art reference cited in the Office Action. It is therefore respectfully requested that claim 1 be allowed and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,

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Enclosures: Replacement Drawings